Session 27 Overview

Image Sensors

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It is estimated that more than 500 million cell-phone cameras and more than 80 million digital still cameras will be sold in 2007. The explosive growth rate of these businesses is being fueled by the development of low-cost high-quality CMOS image sensors. These sensors are being developed by design houses and vertically integrated companies. They are manufactured in both private and publicly available foundries.

The nine presentations in this session represent a snapshot of the recent developments in CMOS image sensors for cell-phone cameras, digital still cameras, HDTV camcorders, and machine vision. It is shown in these papers that the quality of CMOS image sensors is still improving with no clear bound in sight. In addition, the variety of applications for CMOS image sensors is still expanding.

Papers 27.1 and 27.2, present the state-of-the-art in CMOS image sensors for digital still cameras; this include pixel densities greater than 6 million, with pixel sizes less than 2.5μm, and random noise with rms levels less than 8e-. Both of these sensors produce outstanding imagery in both high and low light-level environments.

The next two papers present techniques for improving conversion gain and reducing temporal and fixed-pattern noise in standard 3T active pixel sensors. In Paper 27.3, feedback is used to increase conversion gain by a factor of 5 and reduce reset noise by a factor of 2. Pseudo randomization is used in Paper 27.4 to reduce the peak fixed-pattern noise by more than a factor of 2.

The session continues with two papers that focus on the HDTV market. Paper 27.5 describes a sensor that combines high-speed readout and low-noise operation. It achieves 180 frames per second with 5.2e- rms read noise and 15.9e-/pixel/s dark current at 60°C. Paper 27.6 describes the highest performance analog front-end for HDTV CCD sensors, yet published. It achieves 14-bit 74MS/s performance.

The final three papers present the state of the art in machine vision sensors. In Paper 27.7, the first-published camera-on-a-chip sensor for high-speed industrial cameras is presented. It achieves greater than 1000 frames per second at 516×514 pixel resolution with a standard camera-link interface. Paper 27.8 describes the first-published fully integrated stereo vision sensor that is capable of depth perception at 30 frames per second. It achieves a depth resolution of 0.39m while only consuming 33.6mW. The last paper, Paper 27.9, presents a sensor that is inspired by the human retina. This sensor achieves a dynamic range of greater than 120dB while responding to relative intensity changes in less than 100μs.

27.1 A 1/1.8-inch 6.4MPixel 60frames/s CMOS Image Sensor with Seamless Mode Change **8:30 AM**
S. Yoshihara, Sony, Atsugi, Japan

A 1/1.8-inch 6.4MPixel 60frames/s CMOS image sensor fabricated in a 0.18µm 1P3M process is described. A Zigzag-shaped 1.75T/pixel architecture and a 10b counter-type column parallel ADC enables 2.5×2.5µm² pixels. The resulting pixel has 38% fill factor, 12ke-/lux•s, and random noise of 7e-$_{rms}$. A 10b parallel LVDS interface enables data rates of up to 4.32Gb/s with 216MHz DDR. Full frame and 2×2 binning modes are interchangeable without an extra invalid frame.

27.2 1/2-inch 7.2MPixel CMOS Image Sensor with 2.25µm Pixels Using 4-Shared Pixel Structure for Pixel-Level Summation
Y. Kim, Samsung Electronics, Kiheung, Korea **9:00 AM**

A 1/2-inch 7.2MPixel CMOS image sensor with 2.25µm pixels employs a 4-shared pixel structure with pixel-level charge summation. It achieves a 57% fill factor, full well capacity of 14ke- with 41dB maximum SNR at full resolution, 8e- random noise, 15ke-/lux•s sensitivity, and a 3dB increment in SNR for pixel-level charge summation and sub-sampling operation. A 0.13µm Cu process is used.

27.3 A 3MPixel Low-Noise Flexible-Architecture CMOS Image Sensor **9:30 AM**
J. Yang, Cypress Semiconductor, Cambridge, MA

An image sensor with a 2.54µm pixel fabricated in a 0.18µm CMOS technology is presented. The 3T pixel with drain-side row-select reduces reset noise by cascoded feedback reset and increases responsivity with common-source readout. The reset noise is 13e- and the responsivity at 550nm is 1.12V/lux•s in source-follower readout mode and 5.6V/lux•s in common-source readout mode.

27.4 A CMOS Imager with Column-Level ADC Using Dynamic Column FPN Reduction **9:45 AM**
M. Snoeij, Delft University of Technology, Delft, The Netherlands

A CMOS imager with a column-level ADC uses a dynamic column FPN reduction technique. This technique requires 5 extra switches per column and minimal digital overhead at the chip level while reducing the perceptual effect of column FPN. Measurements show that the prototype makes a column FPN of ±0.67% nearly invisible.

27.5 High-Speed Digital Double Sampling with Analog CDS on Column Parallel ADC Architecture for Low-Noise Active Pixel Sensor **10:15 AM**
Y. Nitta, Sony, Kanagawa, Japan

A progressive 1/1.8-inch 1920×1440 CMOS image sensor with a column-inline dual CDS architecture uses a 0.18µm CMOS process. This sensor implements digital double sampling with analog CDS on a column parallel ADC. Random noise is 5.2e-$_{rms}$ and the DR is 68dB at 180frames/s(6.0Gb/s). FPN is <0.5e-$_{rms}$ without the correction circuit.

27.6 A 14b 74MS/s CMOS AFE for True High-Definition Camcorders **10:45 PM**
R. Kapusta, Analog Devices, Wilmington, MA

A 14b 74MS/s CMOS AFE is designed for true high-definition camcorder applications. This is the first published AFE capable of high-definition sample rates. The AFE operates from a 1.8V supply, achieves 78dB peak SNR, 1.4V input range, and dissipates 70mW.

27.7 CMOS Image Sensor with Integrated 4Gb/s Camera Link Transmitter **11:00 AM**
A. Krymski, Alexima, La Crescenta, CA

A 516×514 1000+ frames/s CMOS sensor with integrated camera link transmitter is designed in 0.35µm 2P3M CMOS and dissipates 1.2W at 3.3V. The sensor can drive a 3m cable delivering 4Gb/s of data.

27.8 A 128×128 33mW 30frames/s Single-Chip Stereo Imager **11:15 AM**
R. Philipp, Johns Hopkins University, Baltimore, MD

A single-chip stereo imager incorporates two 128×128 linear current-mode active pixel sensors with 10µm pixel pitch and 1.2% uncorrected FPN. The chip, fabricated in a 0.35µm 3.3V 4M2P CMOS process, uses parallel computation of the sum-of-absolute-difference matching metric and confidence measures to produce 114×125 depth maps at 30frames/s using 33mW from 3.3V.

27.9 A 128×128 120dB 30mW Asynchronous Vision Sensor that Responds to Relative Intensity Change **11:45 AM**
T. Delbruck, ETH, Zurich, Switzerland

A vision sensor responds to temporal contrast with asynchronous output. Each pixel independently and continuously quantizes changes in log intensity. The 128×128-pixel chip has 120dB illumination operating range and consumes 30mW. Pixels respond in <100µs at 1klux scene illumination with <10% contrast-threshold FPN.